Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS**

1. **Q12**
2. **Q13**
3. **Q14**
4. **Q6**
5. **Q5**
6. **Q7**
7. **Q4**
8. **VSS**
9. **Ø0**
10. **N. Ø0**
11. **Ø1**
12. **RESET**
13. **Q9**
14. **Q8**
15. **Q10**
16. **VDD**

**.080”**

**2**

**1**

**16**

**15**

**11 12 13 14**

**7**

**8**

**9**

**10**

**6 5 4 3**

**MASK**

**REF**

**CD4060BA**

**.069”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VDD**

**Mask Ref: CD4060BA**

**APPROVED BY: DK DIE SIZE .069” X .080” DATE: 4/25/16**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: CD4060B**

**DG 10.1.2**

#### Rev B, 7/1